

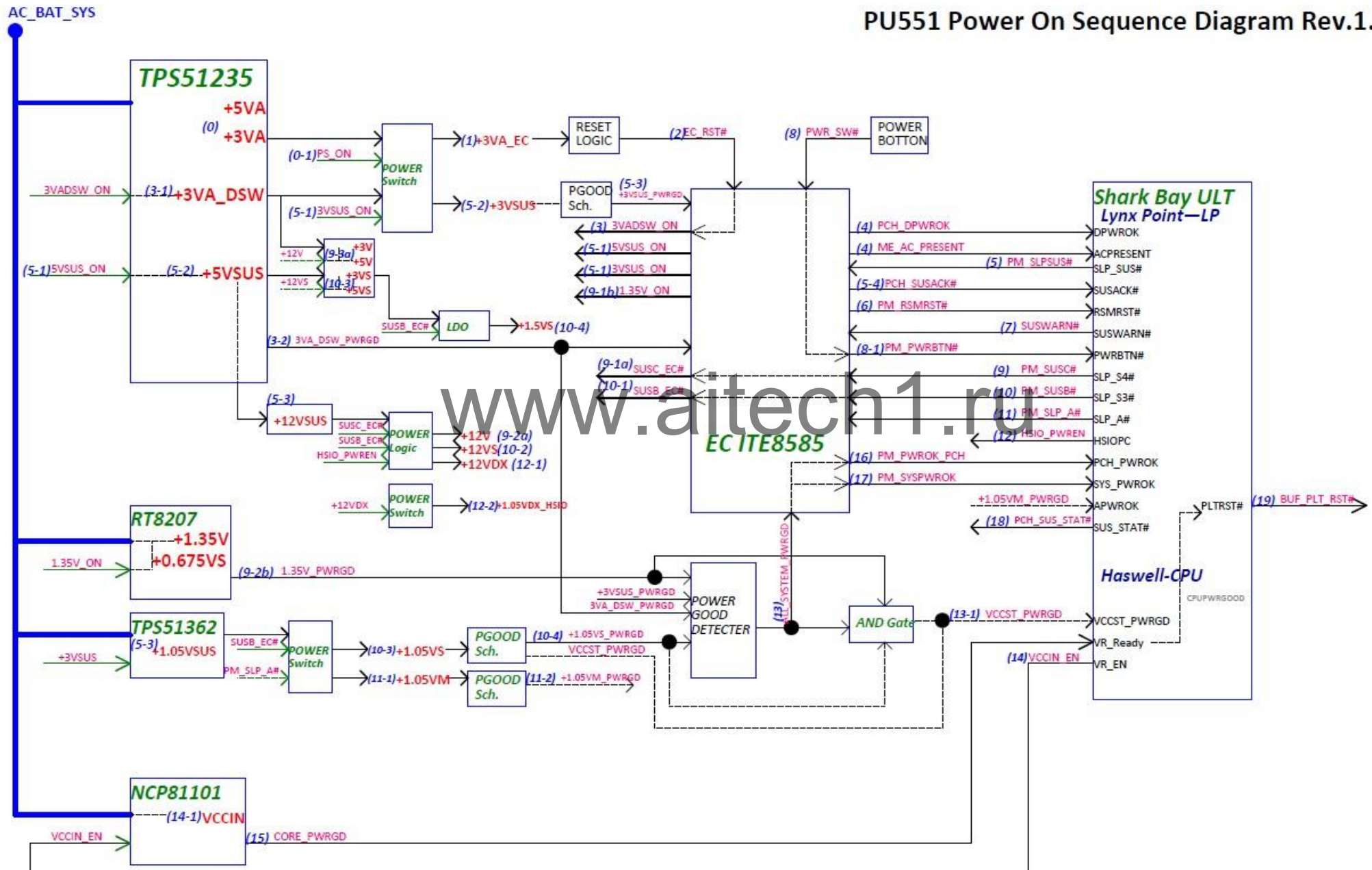
UX305LA SCHEMATIC Revision R2.0

The diagram illustrates the system architecture centered around the **CPU Broadwell ULT** (Page 2-9). The CPU is connected to the **I/O Board** via **LPDDR3 1600MHz** (Page 13-15, 19) and **USB 2.0_I** (Page 62). The I/O Board also includes a **CARDREADER** and an **AUD-CX20752** (Page 36/37). The CPU is connected to the **EC ITE IT8585E LQFP** (Page 50) via **LPC** and **SPI** (Page 20-28). The EC is connected to the **TPM NPCT420AA0W0** (Page 31) and **Debug Conn.** (Page 44). The EC is also connected to the **Charger** (Page 55) via **SMR0** and **SMR1**, and to the **CPU Thermal Sensor** (Page 50) and **DIWM Thermal Sensor** (Page 14) via **SWR1**. The CPU is connected to the **EDP Panel** (Page 48) via **DDI 24** and **DDI**, and to the **HDMI type D** (Page 48) via **DDI 24** and **DDI**. The CPU is also connected to the **Touchpad** (Page 31) via **PS2**. The CPU is connected to the **IO Board** via **USB 2.0_I** and **CARDREADER**. The CPU is connected to the **USB 3.0 PortA** (Page 69) via **USB 3.0_I**.



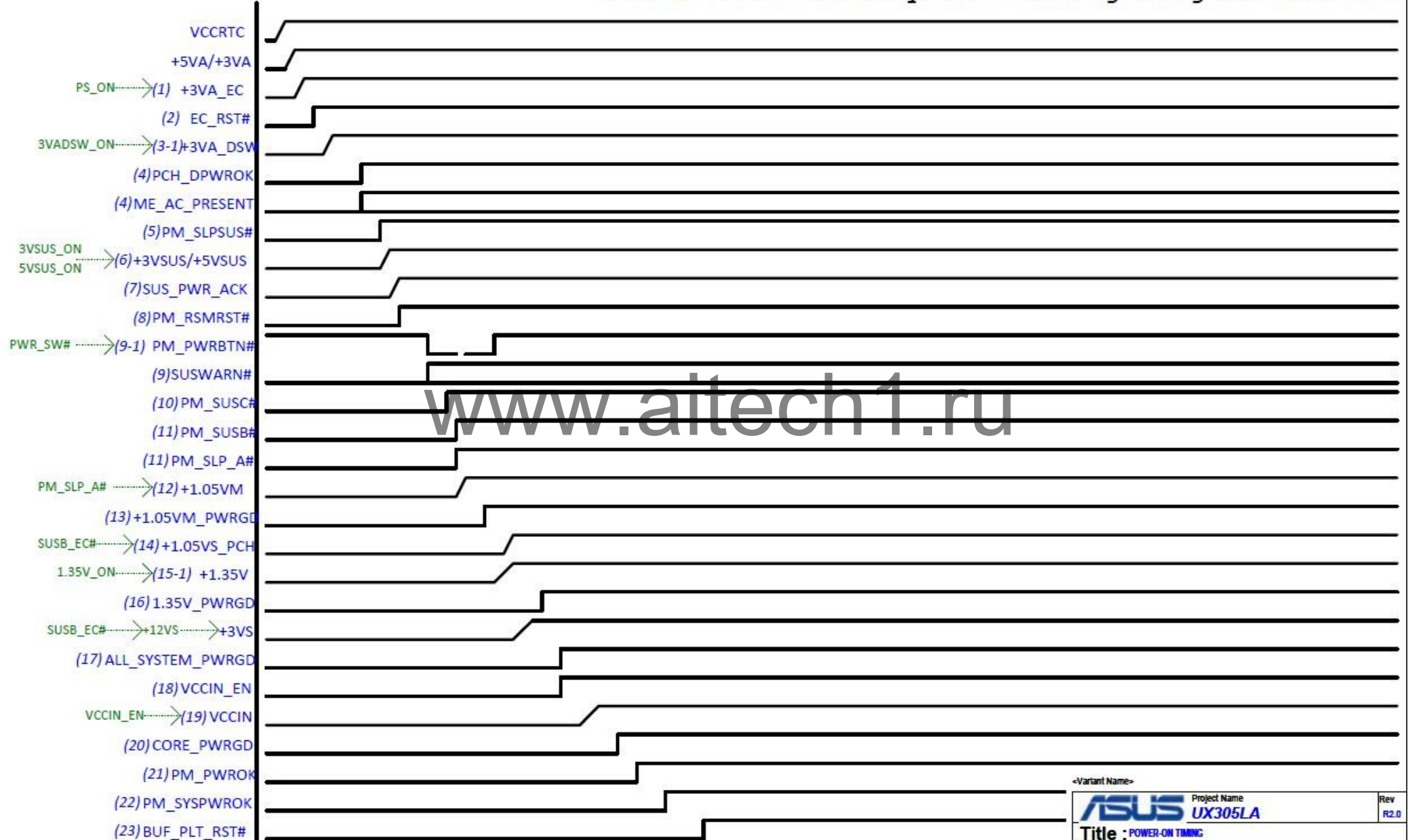
POWER ON SEQUENCE

PU551 Power On Sequence Diagram Rev.1.0



AC mode POWER ON SEQUENCE

BU401 Power-On Sequence Timing Diagram Rev.0.1



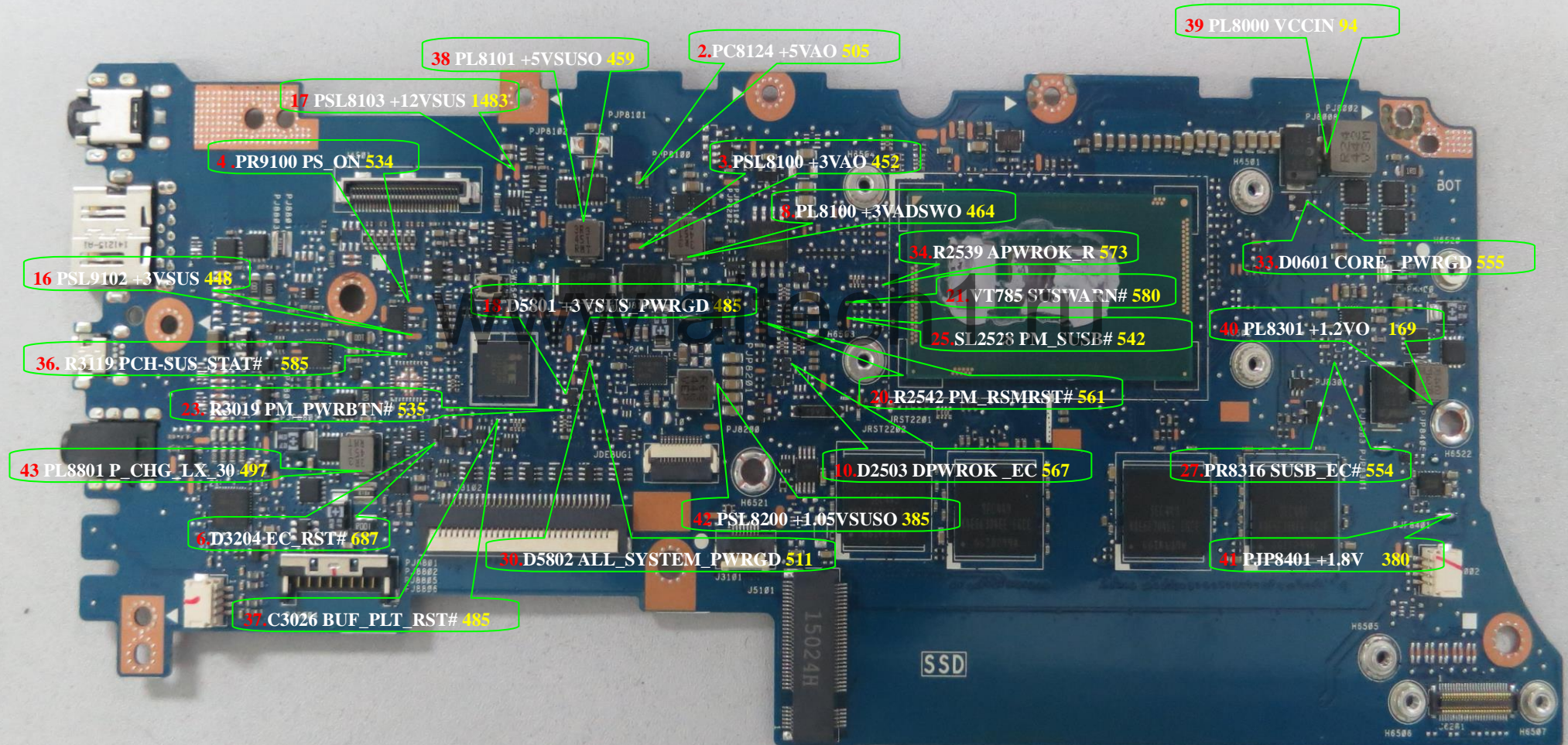
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ASUS Project Name
UX305LA

Rev
R2.0

Title : POWER-ON TIMING

Signal Measure Point-Bottom



Signal Measure Point-Top

